Ross Rogers

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Skills

Languages: C++, Java,Python,javascript, System Verilog, Matlab, Specman, XML, SQL, android,Perl, PHP, bash, make
Software: Linux, gdb, gcc, SAP,Eclipse, Microsoft Visual Studio, Subversion, Git, SCons, VCS, Verdi, Windows

Work Experience

Intel, Software Engineer in Simulation Testbench Infrastructure, March '07 – Present

Knights Landing Super Computing Chip

- Integrated fundamental message passing C++ verification IP into testbench. Improved vendor's reuse flow by transitioning them to git and a more rigorous code patching methodology.
- Supported users on six sites in five different time zones with their usage of the message passing checker and BFM IP.
- Drove simulation performance through weekly profiles using six different profile tools and posted results on the intranet. Implemented refactorings to improve simulation speed by 71%, saving the project ~6 compute years of server time per week of the project.

Knights Corner Super Computing Chip

- Verification technical lead for ring network fabric and distributed cacheline coherency tag directory (DTD). Technical lead in charge of checker infrastructure and coverage-based random sequence testing. Authored ~60% of the verification collateral for these test subjects.
- Identified that build flows were too slow and rewrote the flow in SCons to be 78% faster while supporting modular inheritance-based build derivatives for the 100+ different simulation models on the project. Vastly reduced the size, complexity, and inconsistency of the set of build targets. Enabled parallel building of all steps either locally or on multiple machines. Implemented build flow user feedback in the form of target dependency graphs, report web pages, and build dependency timing diagrams.
- Authored and implemented reuse protocol for sharing verification IP between two projects to avoid forking efforts too early.
- Implemented outlook script to rewrite incomprehensible internal emails into a useful form.
- Authored and supported the network layer of project-critical packet-level modeling and checking infrastructure.

Knights Ferry Super Computing Chip

- Worked as right-hand man of fullchip technical lead to help create and maintain a fullchip testbench for billion gate design. Wrote modeling and cross-checking components in C++, SystemC, and Specman. Created and maintained various memory pre-loading methods and supported hashing and memory interleaving transforms including clarifying and enhancing provided documentation and implementing functions in C++ and Specman for test writers and checker writers.
- Authored checkers for verifying complex interleaved ring-network with virtual channels. Verified the ring-network with random and directed-random tests.
- Used formal verification techniques to validate message class reservations on ring network in order to exhaustively verify specific anti-deadlock properties of the ring network.
- Wrote and maintained python script to convert XML descriptions of control registers into verification components for all control registers in billion-gate chip with a 50 times speed improvement over the previous implementation.

PMC-Sierra, Product Design Engineer, January '06 – February '07

- Responsible for inserting compression DFT logic on 17 blocks. Provided feedback to block designers on testability issues. Scripted DFT logic insertion and test pattern generation flow using Make, Perl, Python, BASH, and Matlab. Improved flow through use of assertions, data parsing, data analysis, and various refactorings. Distributed and maintained flow.
- Verified JTAG functionality on printer chip. Verified RAM BIST functionality through JTAG interface. Scripted mapping of vector re-simulation mis-compares onto original vectors thereby speeding debugging process. Documented and distributed the script.
- Created and simulated functional vectors to test DLL for printer chip. Worked with post-silicon engineers to bring the vectors online.
- Implemented ECO's on printer ASSP per 3rd party's specification. Verified RTL to Pre-Layout and Pre-Layout to Post-Layout netlists using Cadence's formal equivalence tool.

Advanced Digital Information Corporation, EE Intern, Summer 2004 and 2005

- Created test circuits as part of a team for needs of mechanical engineering group. Designed, implemented, tested, and documented connectivity verification circuit for mechanically flexing data/power link to robotic tape manipulator. Designed, implemented, tested, and documented circuitry to exercise solenoid with sensor feedback, RS-232 data logging, and LCD output using Microchip's PIC18F4550 MCU and custom written C code.
- Provided hardware support to the engineering team on the Scalar i500 tape library. Reworked PCBs of the Scalar i500 to implement hardware design changes and repair damaged hardware.
- Tested software and hardware in the firmware test team. Used and refined automation methods involving Perl, IBM's Rational Robot, and in-house programs to stress test the Scalar i500. Documented interaction using *MKS Integrity*.

Education

University of Southern California - MSCS 2013 - Computer Vision, SAP, Web Development
University of Washington - BSEE 2005 - emphases in Digital and Robotics, Dean's List

Research

University of Washington DARPA Grand Challenge Team

- Designed and coded control of relays for basic vehicle actions such as throttle, braking, and turning. Created simple interface to translate control commands to vehicle actions.
- Created test cases and evaluated the performance of obstacle avoidance algorithm as part of a team. Used an assembly level debugger to step through and observe code path.